LINEAR TECHNOLOGY

DESIGN NOTES

Isolated RS485 Transceiver Breaks Ground Loops – Design Note 228

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The RS485 interface standard is designed to handle a –7V to 12V input signal range; however, in practical systems, ground potentials vary widely from node to node, often exceeding the specified range. This can result in an interruption of communications, high current flow through ground loops or worse, destruction of a transceiver. Guarding against large ground-to-ground differentials calls for an isolated interface. A new surface mount device, the LTC®1535 isolated RS485 transceiver, provides a one-chip solution for breaking ground loops and achieving a wide input range.

Previously, isolation was achieved by using at least three optoisolators and a separate isolated power supply. The LTC1535 replaces not only the optoisolators, but also the power supply, as it includes an on-chip DC/DC converter. Other features include selectable driver slew rate to reduce EMI and susceptibility to reflections, full-duplex pinout and fail-safe detection of open and shorted lines.

The LTC1535 consists of two separate dice assembled on a proprietary, isolated lead frame. The lead frame includes integral coupling capacitors that bridge the isolation barrier and exhibit 2,500V_{RMS} guaranteed standoff. Data communication takes place via the coupling capacitors, while an on-chip, 400kHz push-pull converter sends power to the isolated side through a small transformer. Total common mode capacitance across the barrier amounts to less than 20pF, with the transformer accounting for about 16pF of the total. Figure 1 shows the complete circuit for a fully isolated RS485 port.

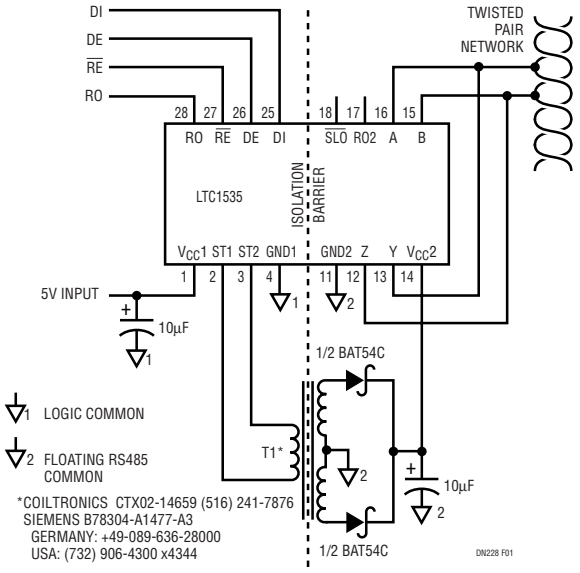

Figure 1. Fully Isolated RS485 Port

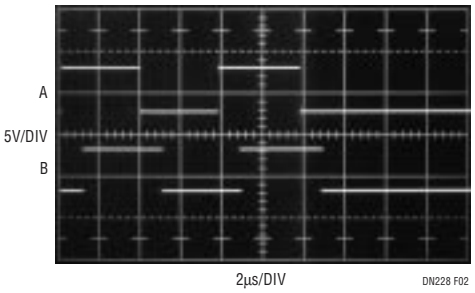

Figure 2. Positive-Going Double-Pulse Behavior: A = Driver Input, B = Receiver Output

Internally, the two halves of the LTC1535 communicate in a ping-pong fashion, first sending transmit data to the isolated side and then sending receive data back to the nonisolated side. The sampling nature of the internal communications link means that some jitter is introduced into the data; this limits the useful baud rate to approximately 500kBd. At 350kBd, the jitter is guaranteed to be less than 10%. Figure 2 shows a double pulse propagating through the LTC1535. Waveform (A) is the transmitter data input and waveform (B) is the output of the receiver. The transmitter and receiver are looped back on the isolated side of the chip. The typical jitter is hardly visible. A negative-going double pulse is shown in Figure 3. The LTC1535 transceiver is unaffected by the DC average of the data waveform. Total round-trip propagation delay through the LTC1535 is approximately 1µs or roughly equivalent to 328 feet of cable.

Figure 4 shows the driver output waveform when loaded by 5000 feet of terminated cable, operating in the fast slew mode (SLO pin pulled high). The effect of the slew pin on

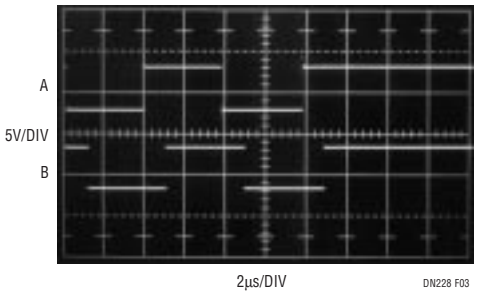

Figure 3. Negative-Going Double-Pulse Behavior: A = Driver Input, B = Receiver Output

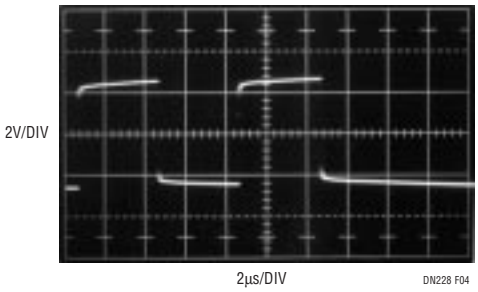

Figure 4. Driver in Fast Slew Mode, Loaded with 5000' of Twice-Terminated Twisted Pair

the driver output waveform is noticeable in Figure 5, where rise and fall times of approximately 1µs result.

The LTC1535 is useful for other types of signal isolation. Figure 6 shows a fully isolated, 24-bit differential input A/D converter implemented with the LTC1535 and LTC2402. Power on the isolated side is regulated by an LT1761-5 low noise, low dropout micropower regulator. Its output is suitable for driving bridge circuits and for ratiometric applications.

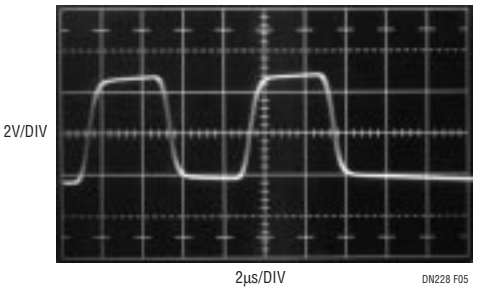

Figure 5. Driver in Slow Slew Mode, Loaded with 5000' of Twice-Terminated Twisted Pair

During power-up, the LTC2402 becomes active at V_{CC} = 2.3V, while the isolated side of the LTC1535 must wait for V_{CC2} to reach its undervoltage lockout threshold of 4.2V. Below 4.2V, the LTC1535's driver outputs Y and Z are in a high impedance state, allowing the 1kΩ pull down to define the logic state at SCK. When the LTC2402 first becomes active it samples SCK; a logic "0" provided by the 1kΩ pull-down invokes the external serial clock mode. In this mode the LTC2402 is controlled by a single clock line from the nonisolated side of the barrier, through the LTC1535's driver output Y. The entire power-up sequence, from the time power is applied to V_{CC1} until the LT1761's output has reached 5V, is approximately 1ms.

Data returns to the nonisolated side through the LTC1535's receiver at RO. An internal divider on receiver input B sets a logic threshold of approximately 3.4V at input A, facilitating communications with the LTC2402's SDO output without the need for any external components. For further details of the LTC2402's logic interface and serial output bit stream, see the LTC2402 data sheet.

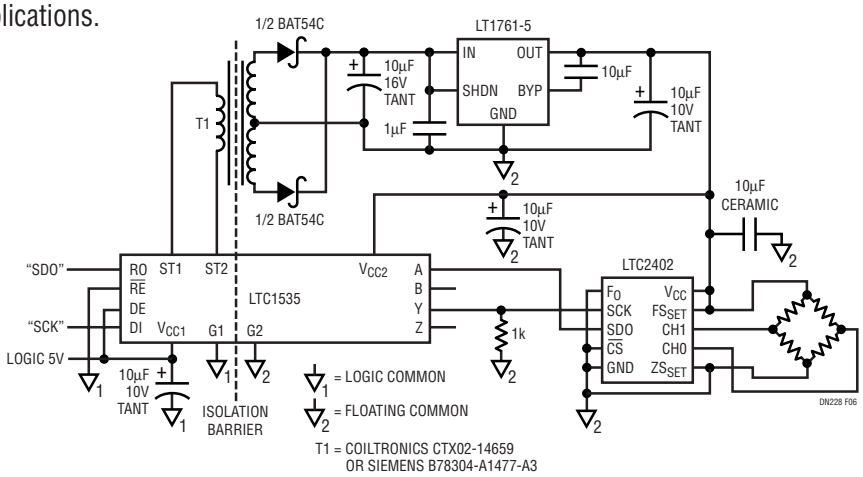

Figure 6. Complete Isolated 24-Bit Data Acquisition System

Data Sheet Download

http://www.linear-tech.com/go/dnLTC1535

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